REMARKS

Claims 1-8 and 10-19 are pending in the present application. Claims 9 and 20 were previously cancelled. Claims 1-8, 10, 12-19 have been amended herein. No new matter has been added by these amendments. Applicants have also submitted a replacement specification and replacement drawings.

Examiner Interview:

On February 21, 2007, Applicants' attorney, Michael J. Fogarty, III and USPTO Examiner Cynthia Britt participated in a telephonic interview. The parties discussed the specification, drawings, and claims and proposed amendments thereto. It was agreed that Applicants would submit amendments to the specification and drawings consistent with the Examiner's suggestions in the Office Action. Applicants also agreed to submit amended claims for the Examiner's consideration. Applicants' attorney thanks the Examiner for her time and comments during the interview.

Replacement Drawings:

Applicants' previously submitted replacement drawings have been objected to and the Examiner has requested that descriptive labels other than numerical labels be added to Figures 1-5. Applicants have submitted a new set of replacement drawings herewith. Additional labels have been added to the elements of Figures 1-5. Additionally, Figures 1, 2 and 4 have been labeled as prior art. No new matter has been added to the application by these amendments to the drawings. The text added to the Figures is supported in the original specification at paragraphs [0023] – [0028].

Replacement Specification:

As suggested by the Examiner, Applicants have submitted a replacement specification to correct text translated from a parent German patent application. Applicants are submitting herewith a clean and marked-up copy of the replacement specification. The term "useful data" has been changed to "user data" and the term "memory checking device" has been changed to "memory control device" throughout for clarification. The present application claims priority to a German application and was derived from a translation of the priority document. With respect to the term "useful data," the German parent application uses the term "Nutzdaten," which can more clearly be translated as "user data" or "utility data." Further, the term "memory checking device" can be more clearly translated as "memory control device," which is derived from the German term "Speicherkontrolleinrichtungen" in the priority German application. The substitute specification includes no new matter.

Applicants have clarified the description of Figures 1, 2 and 4 to note that the drawings are illustrating prior art devices. Applicants have also amended the Summary in paragraph [0021] to clarify the bus configuration language discussed during the Examiner interview.

Claim Objections and Rejections:

Claims 15 and 19 have been objected to due to informalities. Applicants have amended claims 15 and 19 to address the issues raised in the Examiner's objections.

Claims 18 and 19 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the Applicants regard as the invention. Applicants have amended claims 15 and 19 to clarify the claim terms cited by the Examiner.

Claims 1-8 and 10-19 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Applicants' Admitted Prior Art (AAPA) in the background of the present application. Applicants respectfully traverse these rejections.

Applicants' Admitted Prior Art, which is discussed in connection with Figures 1, 2 and 4 of the disclosure, requires that each memory module has separate data memory devices for redundancy data and buffer/redriver modules. See original disclosure at paragraphs [0017] – [0020] and [0030]. Pending independent claims 1, 12, and 17 require a buffer and error checking module that is combined into a single device on the memory module. The integrated buffer and error checking module includes both buffer/retriever circuitry and DRAM circuitry for storing error correction data transmitted from the memory controller to the memory module. Integrating the error correction data DRAM circuitry and the buffer circuitry in the same module saves space on the memory module. Additionally, the circuit paths between a pure buffer/retriever device and error correction data DRAM circuitry may be eliminated in the memory module using the present invention. The prior art memory modules do not teach or suggest these features of the pending claims. Applicants respectfully request that the Examiner withdraw the rejection under 35 U.S.C. § 102(e) and pass the claims to issue.

Claims 2-8, 10, 11, 13-16, 18 and 19 depend from claims 1, 12 and 17, respectively, and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Michael J. Fogarty, III, Applicants' attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. The RCE fee under 37

C.F.R. 1.17(e) is required by 37 C.F.R. 1.114. The Commissioner is hereby authorized to charge, or credit any overpayment, Deposit Account No. 50-1065.

Respectfully submitted,

3/12/2007
Date

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